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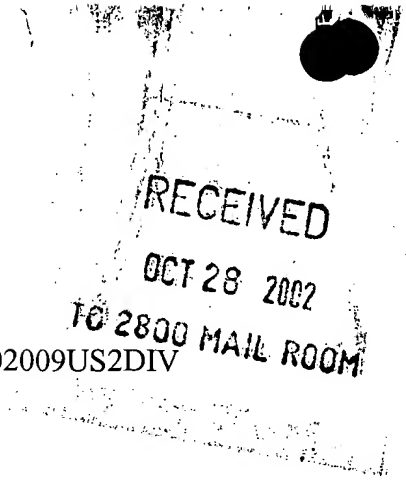

DOCKET NO: 202009US2DIV

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COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

RE: U.S. Application
Serial No: 09/761,738
Filed: January 18, 2001
Inventor: Shigenobu MAEDA
For: Manufacturing Method of Semiconductor . . .

SIR:

Attached hereto for filing are the following papers:

REPLY BRIEF w/ APPENDIX I (IN TRIPLICATE)
REQUEST FOR ORAL HEARING

Our check in the amount of $ --280.00-- is attached covering any required fees. In the event that any variance exists between the amount enclosed and the Patent Office charges for filing the above-noted documents, including any fees required under 37 CFR 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, please charge or credit our Deposit Account No. 15-0030. Further, if these papers are not considered timely filed, then a petition is hereby made under 37 C.F.R. 1.136 for the necessary extension of time. A duplicate copy of this sheet is attached.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

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#12/Oral Hearing

Docket No. 202009US2DIV

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: SHIGENOBU MAEDA

GAU: 2824

SERIAL NO: 09/761,738

EXAMINER: LEBENTRITT, M.

FILED: JANUARY 18, 2001

FOR: MANUFACUTRING METHOD OF SEMICONDUCTOR WAFER, SEMICONDUCTOR . . .

REQUEST FOR ORAL HEARING

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Applicant's representative hereby respectfully requests that an Oral Hearing be scheduled in the above-identified application.

A check in the amount of **$280.00** to cover the fee is enclosed herewith and any further charges may be made against the Attorney of Record's Deposit Account No. **15-0030**. A duplicate copy of this sheet is enclosed.

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: :

SHIGENOBU MAEDA : EXAMINER: LEBENTRITT, M.

SERIAL NO: 09/761,738

FILED: JANUARY 18, 2001 : GROUP ART UNIT: 2824

FOR: MANUFACTURING METHOD OF SEMICONDUCTOR WAFER, . . .

REPLY BRIEF UNDER 37 C.F.R. §1.193

ASSISTANT COMMISSIONER OF PATENTS
WASHINGTON, DC 20231

SIR:

This is a Reply to the Examiner's Answer mailed August 30, 2002. An Appeal Brief was timely filed on July 22, 2002.

REPLY TO EXAMINER'S ANSWER

As described in the Appeal Brief, Appellant's invention is directed to a method of manufacturing a semiconductor device. As described in the specification, the field of semiconductor device manufacturing has experienced a recent trend in that circuit components or elements called "intellectual properties" are being combined into highly integrated circuits.[1] Each of the intellectual properties is itself a large scale integrated circuit composed of many circuit elements combined to provide an overall function for the intellectual property.[2] However, conventional semiconductor device manufacturing

[1]Specification at page 2, line 22-page 3, line 2.

[2]Id.

techniques are inflexible and allow the mass production of relatively few kinds of highly integrated circuits, making profits difficult to realize in the integrated circuit manufacturing industry.[3] The present invention is directed to a flexible system for manufacturing semiconductor devices that allows the mass production of several kinds of highly integrated circuits.[4]

THE FIRST ISSUE

The term "intellectual properties" in Claims 21 and 22 is not indefinite under 35 U.S.C. §112, second paragraph.

Appellant's Brief presented two Internet web sites as evidence that "intellectual property" can mean a predefined circuit that can be formed on a semiconductor wafer as a component of a larger operational circuit. While the Examiner's answer acknowledges that these web sites indicate that there is more than one accepted meaning of the term "Intellectual property," the Answer asserts that the web sites do not support Appellant's intended meaning. Appellant disagrees with this assertion. Taking the www.mentor.com site as an example, the "about IP" link of this site discusses the design and reuse of third party Intellectual Property in the context of reusable cores such as encoders, decoders, bus interfaces, processors etc.[5] Moreover, the "IP viewpoint" and "IP Remarketing Program" links of this site makes clear that "intellectual properties" are pre-designed reusable blocks of semiconductor circuits that are used to produce larger application specific systems.[6] Thus, it is clear from the

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[3]Specification at page 3, lines 3-10.

[4]Specification at page 9, lines 11-12.

[5]Appendix I at page 1, lines 1-10. Appendix I attached hereto includes consecutively number pages printed from the www.mentor.com site.

[6]Appendix I at page 2, lines 12-27; page 4, lines 1-8.

www.mentor.com Internet site that "Intellectual Properties" can be predefined circuits that can be formed on a semiconductor wafer as a component of a larger operational circuit. This meaning is further supported by the "IP Evaluation" link of the www.mentor.com site, which lists 27 functional circuits as "IPs" available for evaluation.[7]

In response to Appellant's argument that the term "intellectual properties" is defined in the specification with sufficient clarity to enable one of ordinary skill in the art to reasonably ascertain the scope of the claim, the Examiner's answer take the position that the scope of this term is indefinite in the specification itself. In support of this position, the Answer lists numerous examples provided in the specification of circuits of varying complexity that can be Intellectual Properties, and apparently asserts that these examples make the term Intellectual Properties indefinite in the specification. However, as noted in Appellant's Brief, the specification reads as follows:

> This is followed by a move afoot to form a highly integrated circuit by combining various circuit components (referred to as "microcells" or "IP (Intellectual Property)"), each composed of circuit elements and performing a certain function.[8]

Thus, the specification defines IP as a circuit component composed of circuit elements and which performs a certain function; this meaning is completely consistent with each of the examples of IPs given in the specification and list in the Examiner's Answer.

Finally, in support of the assertion that Appellant's intended meaning of "Intellectual Properties" is repugnant to the accepted meaning of this term, the Examiner's Answer cites page 5, line 21 of the Appeal Brief as an admission by Appellant that the accepted meaning of

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[7]Appendix I at page 5.

[8]Specification at page 2, line 24 - page 3, line 2.

Intellectual Property is "the intangible creations of the human intellect that are protected by law." However, this cited portion of the Appeal Brief makes no such admission, but rather attributes the statement of accepted meaning to the Final Action. While Appellant acknowledges that the Final Action's asserted accepted meaning is one meaning of "Intellectual Properties," Appellant maintains the position that Appellant's use of this phrase is consistent with semiconductor industry accepted meaning for this term and is also consistent with the Final Action's asserted accepted meaning of this term. To reiterate, one can easily understand how "Intellectual Property" may be used to describe a functional circuit because such circuits frequently embody "intangible creations of the human intellect that are protected by law."

For the reasons stated above, the rejection under 35 U.S.C. §112, second paragraph, should be reversed.

THE SECOND ISSUE

Krolikowski et al. does not teach arranging each mask pattern of the plurality of intellectual properties for a layout pattern as recited in Claim 21.

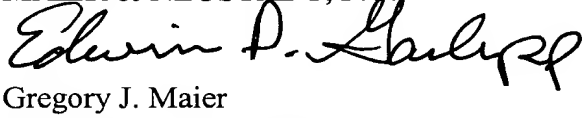
The Answer also argues that Krowlikowski et al's method of fabricating an FET memory chip discloses the claimed step of arranging each mask pattern of plural intellectual properties for a layout pattern. In support of this position, the Answer apparently takes the position that the FETs on the chip are intellectual properties having a gate, source and drain as elements. However, as noted above, intellectual properties are ***circuits*** that include a plurality of ***circuit elements*** to perform a certain function. Appellant submits that one of ordinary skill in the art would not consider an FET as a "circuit," or the source, gate and drain

of the FET as "circuit elements," and therefore would not consider the FET as an Intellectual Property. Therefore, Claim 21, and Claims 22-24 which depend therefrom, patentably define over Krolikowski et al.

For the reasons stated above, Appellant maintains its position that Claims 21-24 meet the requirements of 35 U.S.C. §112, second paragraph, and that the prior art neither discloses nor suggests the method of manufacturing a semiconductor device as recited in Claims 21-24. Accordingly, it is respectfully requested that all the rejections still pending in the final Office Action be REVERSED.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



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APPENDIX I

Inventra Mentor Graphics IP Division

Whether designing the latest in complex electronic consumer and communication technologies or trying to meet increasingly tighter time-to-market windows, ASIC and IC designers are faced with the necessity of design reuse a third party intellectual property. Sourcing standard and application specific functions from independent Intellectual Property (IP) developers enables ASIC and IC designers to concentrate on optimizing system architecture and developing proprietary functionality.

Mentor Graphics Inventra IP Division provides an expansive array of reusable cores for a broad range of consume digital, computing, networking and communication applications. Inventra's offering includes DSP processors, Viterl Reed-Solomon encoders/decoders, audio codecs, bus interfaces, processors, micro-controllers, Ethernet, ATM an Sonet data communication cores.

All soft cores are available in Verilog and/or VHDL, which can be synthesized and targeted to any foundary proces choice. Inventra soft cores also support tool flow from all leading EDA vendors.

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Viewpoint

By Walden C. Rhines, President and CEO, Mentor Graphics Corporation

Until now, the entire electronics industry has been fueled by the relentless march of IC technology, which continues to double the transistor count on a single chip every 18 montl Logic designers, once handicapped by a lack of real estate to house their designs, are nov to install their wildest dreams on a solitary piece of silicon. Along the way, computer syster have shrunk from mainframe monsters to desktop systems to devices that now fit easily in palm of your hand.

But now, as the industry moves into the submicron era, we are facing a crisis that is turning designers' dreams into potential nightmares. Suddenly, engineers are sailing in an ocean of IC gates so vast that t are losing sight of the shore. With upwards of 50 million transistors on a typical chip by the year 2000, i take 75 designers an entire year to create the hardware to fill it with meaningful functionality.

Clearly, the time has come for a significant shift in design methodology, and at the heart of this shift is t principle of design reuse. The only efficient way to create sub-micron ICs is to employ large blocks that been previously designed, and then to integrate these blocks into an ASIC architecture which also inclu new design blocks, representing true innovation on the part of the design team. This way, the team car focus on areas of the architecture where it truly adds value in terms of the product's target market, and the rest to pre-designed blocks that deliver the more routine functions in a predictable manner.

But where will these pre-designed blocks come from? How will you modify them to work in a new desig Will they work with your current EDA tools? What fab facilities will support them?

Welcome to the emerging world of intellectual property, where hardware designers are presented with a almost overwhelming set of options when it comes to acquiring and implementing both "hard" and "soft" macros as reusable blocks in their designs. At Mentor Graphics, we believe the impact of intellectual property on ASIC and IC design will be so profound that we have established a separate Intellectual Property Business Unit whose sole charter is to provide our customers with comprehensive solutions tc enable the resale, reuse and support of intellectual properties. As a result, we are keenly aware of both challenges and the promise of this new methodology.

Below you'll find viewpoints from two respected journalists, Ron Wilson and Jonah McLeod, who prese their thoughts on the future of intellectual property. It's a great introduction to a subject that will be with for some time to come.

By Ron Wilson, Managing Editor for Semiconductors, EE Times
If someone tries to break into the design process at a new point, the result will be an inefficient, joint-development type of relationship between the designer and the vendor until tools and standards actuall support a hands-off interface at that point. It has only been recently, for instance, that improvements in and route, extraction and checking tools have made customer-owned tooling practical for more than a f sophisticated customers. Now it is an increasing part of the business.

The alleged Intellectual Property revolution needs to be seen in these terms as well. It is nothing more an attempt to break the design process at yet another point, this time between the requirements definiti and the circuit design. Decide what you need, the IP provider says, and we will provide blocks which yc can simply stitch together to create your circuit design.

This new attempt to create a competitive market -- this time for reusable circuit designs -- will follow the same pattern as previous attempts. At the moment, neither tools nor standards support the partition be requirements and circuit design. There is profound confusion about how to represent large IP blocks at behavioral level, how to simulate them, in what format to deliver them, and what additional information needs to accompany the formal definition of the block. Consequently, as in previous examples, attempt use third-party IP quickly come to resemble joint-development contracts rather than purchases of components. This is inefficient to both the would-be consumer and the would-be provider, as both end doing a lot more work than they had in mind.

It is reasonable to assume that both tools and standards will evolve -- probably in a de facto way -- to s these problems. But history suggests the evolution will not be quick, and will not be particularly hurried attempts of industry groups to push it. In the meantime, we will see a gradual shift in the use of IP, from today's norm of relationships that look like involuntary partnerships, to something more resembling a components market. The shift will proceed unevenly, starting with relatively simple digital libraries and proceeding, eventually, through processors, application-specific DRAM and mixed-signal blocks.

By Jonah McLeod, Editor in Chief, Integrated System Design
Just as today a designer can buy standard packaged components from a variety of semiconductor ven and put them on a common printed circuit board, in the future the same will be true of cores. Today, intellectual property exists in a variety of types: hard, soft, and firm, each with its own advantages and disadvantages.

The advantage to hard layout is small size, high performance and other optimization such as low powe Another plus is the designer knows the timing across the core since gates and interconnect have been specified. One drawback is that the core must be used as-is with no changes. Another is the designer i limited in where he can fab his larger design if he uses the core.

Firm cores offer a bit more flexibility in that they exist as optimized, synthesized netlists. Their advanta they can be optimized for timing during final place and route. However, the core cannot be combined w surrounding logic to reduce total design gate count. Soft cores offer the greatest flexibility since they ar supplied in the form of high-level description language that can be synthesized with surrounding logic. it can be optimized during synthesis to reduce gate count and achieve some desired level of performan versus area.

However, its inherent flexibility is also its disadvantage since the co-mingled logic of the soft core must verified along with the surrounding logic. Developing a test bench to achieve this result is the most diffi part of using a soft core.

Beyond the technical problem of each of these IP types is an even more overriding problem, a commor industry-standard interface for exchanging the cells. That's the goal of the Virtual Socket Interface, or V Alliance, formed in September of 1996 by more than 35 major semiconductor, EDA and IP vendors.

The alliance aims to form the Virtual Socket Interface (VSI) that will allow "virtual components" from dif suppliers to be mixed on a single IC substrate. VSI will provide the common interface standard that will IP to fit into virtual sockets at the functional bus interface protocol level or the lower physical clock, test power level.

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WHY?

In the ever more complex world of SoC (system-on-chip), product developers recognize the impracticality of designing all necessary functional blocks internally. Recognizing our customers need to have quick access to reusable IP blocks from a variety of IP sources, Mentor Graphics has become a recognized leader in remarketing Reusable IP.

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HOW?

Inventra IP is either internally created at Mentor Graphics or provided by other companies or customer who wish to place their IP in the Mentor Graphics Inventra Library. Much of the IP remarketed by Inver will originate from semi-conductor companies, system houses and independent third-party IP providers

Benefits to Our Customers

- Access to the broadest range of IP in the industry
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- Worldwide promotion and distribution of your IP in Inventra's Library of Cores
- Sales leverage due to availability of complementary IP from yet other providers
- Standardized quality and delivery mechanisms

Mentor Graphics realizes that no one company can create all of the IP needed today for system-on-chi (SoC) design. The Mentor Graphics IP Third Party Remarketing Program has been designed to solve t problem. We can offer this program to emerging, as well as established IP creators and design compa the leverage to get it all.

If you are interested in participating in Mentor Graphics' IP Remarketing Program, please complete ou Remarketing Submission Form.

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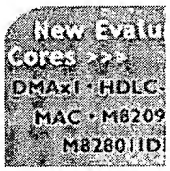

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